



# Applications Note: SY5002C

## Flyback Controller

### With Primary Side CV/CC Control For Adapters and Chargers

### General Description

SY5002C is a single stage Flyback controller targeting at Constant Current / Constant Voltage (CC/CV) applications. Both current and voltage regulation are achieved by primary side control technology for low cost application. To achieve higher efficiency and better EMI performance, SY5002C drives Flyback converters in the Quasi-Resonant mode and adaptive PWM/PFM control. In addition, SY5002C has cable compensation to regulate the output voltage for better load regulation at cable terminal.

### Ordering Information

SY5002C□(□□)□  
 └───┬───┬───  
 Temperature Code  
 Package Code  
 Optional Spec Code

Ordering Number	Package type	Note
SY5002CABC	SOT23-6	----

### Features

- Primary side CV/CC control eliminates the opto-coupler.
- Valley turn-on of the primary MOSFET to achieve low switching losses
- Internal CC/CV loop compensation
- The self-adaption compensation for better stability
- PWM/PFM control for higher average efficiency
- Fast dynamic load transient response
- Cable compensation for better load regulation
- Low start up current: 4μA Max
- Reliable protections for OVP, SCP, OTP
- Reliable protections for safety requirement
- Maximum switching frequency limitation 125kHz
- Compact package: SOT23-6

### Applications

- AC/DC adapters
- Battery Chargers

### Typical Applications

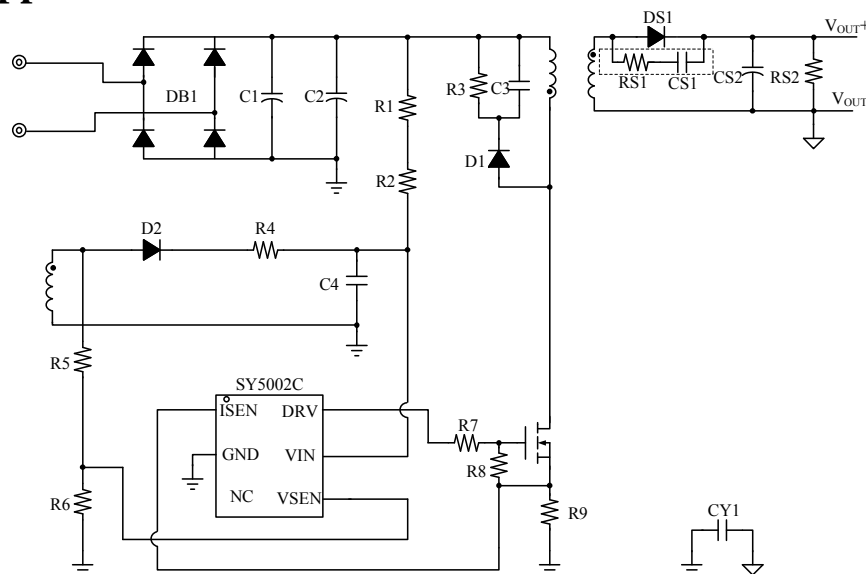
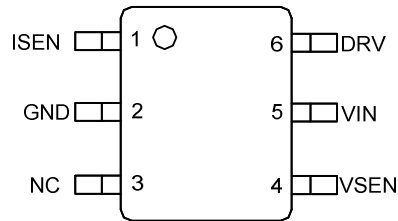


Figure 1. Schematic Diagram

**Pinout** (top view)



**(SOT23-6)**

**Top Mark:** ZSxyz (device code: ZS, x=year code, y=week code, z= lot number code)

Pin	Name	Description
1	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
2	GND	Ground pin.
3	NC	Not used
4	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
5	VIN	Power supply pin.
6	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET.

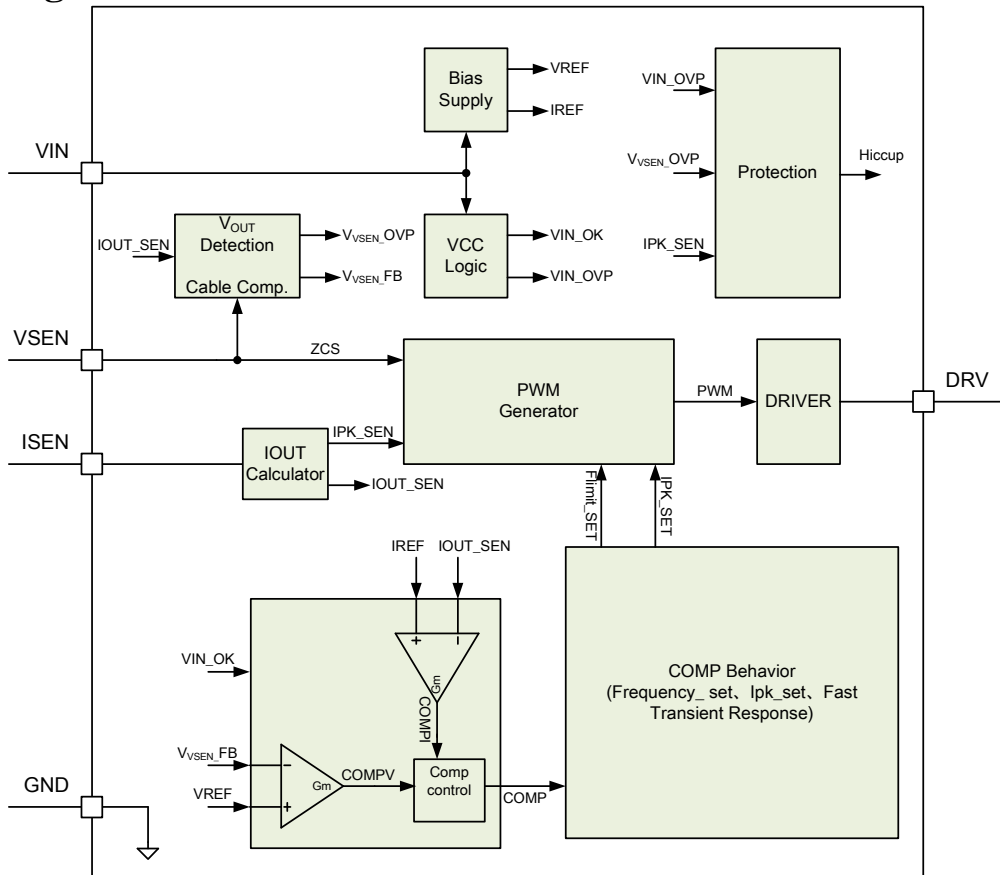
## Absolute Maximum Ratings (Note 1)

VIN	-0.3V~21V
DRV	-0.3V~15V
Supply Current I <sub>VIN</sub>	20mA
ISEN, COMP	-0.3V~3.6V
VSEN	-0.3V~V <sub>VIN</sub> +0.3V
Power Dissipation, @ T <sub>A</sub> = 25°C SOT23-6	0.6W
Package Thermal Resistance (Note 2)	
SOT23-6, θ <sub>JA</sub>	170°C/W
SOT23-6, θ <sub>JC</sub>	130°C/W
Temperature Range	-45°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

## Recommended Operating Conditions (Note 3)

VIN, DRV	9V~17.5V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 105°C

## Block Diagram





## Electrical Characteristics

( $V_{IN} = 12V$  (Note 3),  $T_A = 25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Power Supply Section</b>						
VIN turn-on threshold	$V_{VIN,ON}$			14.7		V
VIN turn-off threshold	$V_{VIN,OFF}$			7		V
VIN OVP voltage	$V_{VIN,OVP}$			17.5		V
Start up Current	$I_{ST}$	$V_{VIN} < V_{VIN,OFF}$			4	$\mu A$
Operating Current	$I_{VIN}$	$C_L = 500pF, f = 100kHz$		1		mA
Quiescent Current	$I_Q$	$CL=0, f=2kHz$		200		$\mu A$
Shunt current in OVP mode	$I_{VIN,OVP}$	$V_{VIN} > V_{VIN,OVP}$		7.5		mA
<b>Current feedback modulator Section</b>						
Internal reference voltage	$V_{REF}$		-1.5%	0.42	+1.5%	V
<b>ISEN Sense Section</b>						
Current limit reference voltage	$V_{ISEN,LIM}$	$V_{FBV} < 0.4V$		0.7		V
		$V_{FBV} > 0.4V$	-5%	1	+5%	V
Latch Voltage for ISEN	$V_{ISEN,EX}$			2		V
<b>VSEN pin Section</b>						
OVP voltage threshold	$V_{VSEN,OVP}$		-5%	1.45	+5%	V
VSEN pin voltage reference	$V_{VSEN,REF}$		-1.5%	1.25	+1.5%	V
Cable Compensation coefficient	$K_3$			17.5		$\mu A/V$
<b>Gate Driver Section</b>						
Gate driver voltage	$V_{Gate}$			12		V
Maximum source current	$I_{SOURCE,MAX}$			120		mA
Maximum sink current	$I_{SINK,MAX}$			500		mA
Max ON Time	$T_{ON,MAX}$			24		$\mu s$
Min ON Time	$T_{ON,MIN}$				300	ns
Max OFF Time	$T_{OFF,MAX}$			500		$\mu s$
Min OFF Time	$T_{OFF,MIN}$			1.2		$\mu s$
Maximum switching frequency	$f_{MAX}$			125		kHz
<b>Thermal Section</b>						
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3:** Increase VIN pin voltage gradually higher than  $V_{VIN,ON}$  voltage then turn down to 12V.

## Operation

SY5002C is a high performance Flyback controller with primary side control and constant current and constant voltage regulation.

The Device provides primary side control to eliminate the opto-isolators or the secondary feedback circuits, which would cut down the cost of the system.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which turn ON the power MOSFET when the voltage across Drain and Source is at its lowest point; the start up current of the device is rather small (4μA typically) to reduce the standby power loss further.

In order to improve the stability, the self-adaption compensation is applied.

The device provides reliable protections such as Over Voltage Protection (OVP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection , VSEN pin short protection ,etc..

SY5002C can be applied in AC/DC adapters, Battery Chargers and other consumer electronics.

SY5002C is available with SOT23-6 package.

## Applications Information

### Start up

After AC supply or DC BUS is powered on, the capacitor  $C_{VIN}$  across VIN and GND pin is charged up by BUS voltage through a start up resistor  $R_{ST}$ . Once  $V_{VIN}$  rises up to  $V_{VIN\_ON}$ , the internal blocks start to work.  $V_{VIN}$  will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain  $V_{VIN}$  above  $V_{VIN\_OFF}$ .

The whole start up procedure is divided into two sections shown in Fig.2.  $t_{STC}$  is the  $C_{VIN}$  charged up section, and  $t_{STO}$  is the output voltage built-up section. The start up time  $t_{ST}$  composes of  $t_{STC}$  and  $t_{STO}$ , and usually  $t_{STO}$  is much smaller than  $t_{STC}$ .

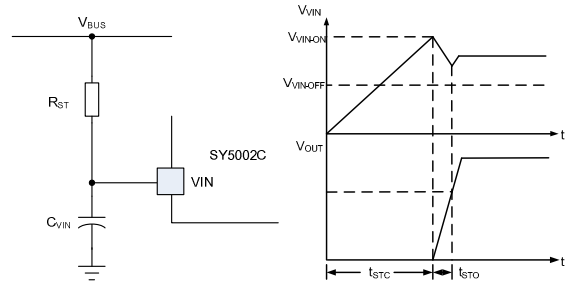


Fig.2 Start up

The start up resistor  $R_{ST}$  and  $C_{VIN}$  are designed by rules below:

(a) Preset start-up resistor  $R_{ST}$ , make sure that the current through  $R_{ST}$  is larger than  $I_{ST}$  and smaller than  $I_{VIN\_OVP}$

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where  $V_{BUS}$  is the BUS line voltage.

(b) Select  $C_{VIN}$  to obtain an ideal start up time  $t_{ST}$ , and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the  $C_{VIN}$  is not big enough to build up the output voltage at one time. Increase  $C_{VIN}$  and decrease  $R_{ST}$ , go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

### Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin,  $V_{VIN}$  will drop down. Once  $V_{VIN}$  is below  $V_{VIN\_OFF}$ , the IC will stop working.

### Quasi-Resonant Operation(valley detection)

QR mode operation provides low turn-on switching losses for Flyback converter.

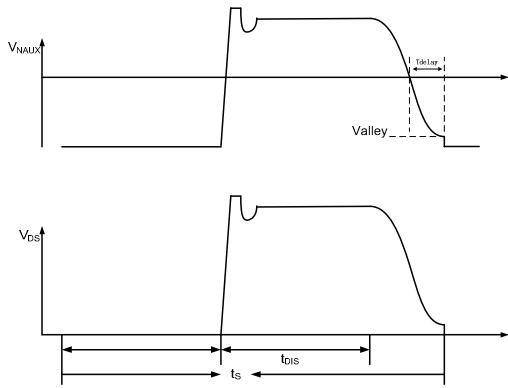


Fig.3 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

**Output Voltage Control(CV control)**

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

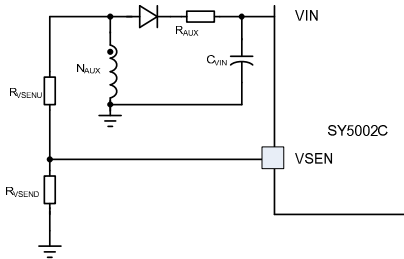


Fig.4 VSEN pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D-F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

$N_{AUX}$  is the turns of auxiliary winding;  $N_S$  is the turns of secondary winding;  $V_{D-F}$  is the forward voltage of the power diode.

At the current zero-crossing point,  $V_{D-F}$  is nearly zero, so  $V_{OUT}$  is proportional with  $V_{AUX}$  exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN-REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where  $V_{VSEN-REF}$  is the internal voltage reference.

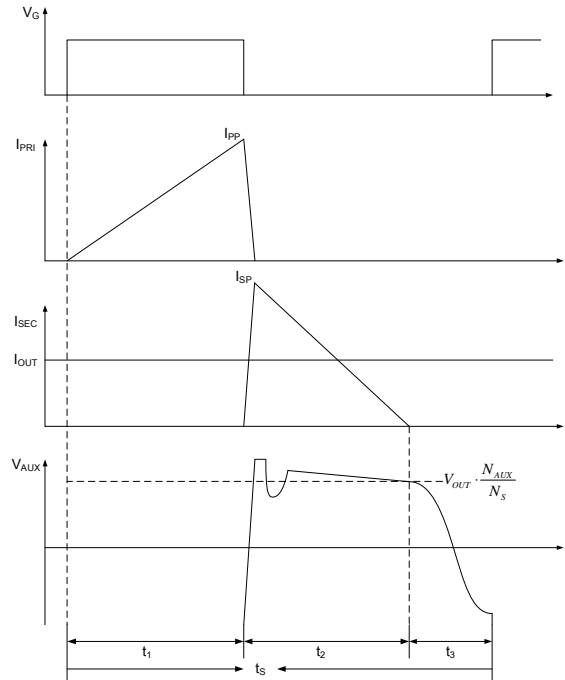


Fig.5 Auxiliary winding voltage waveforms

**Output Current Control(CC control)**

The output current is regulated by SY5002C with primary side detection technology, the maximum output current  $I_{OUT-LIM}$  can be set by

$$I_{OUT-LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where  $k_1$  is the output current weight coefficient;  $V_{REF}$  is the internal reference voltage;  $R_S$  is the current sense resistor.

$k_1$  and  $V_{REF}$  are all internal constant parameters,  $I_{OUT-LIM}$  can be programmed by  $N_{PS}$  and  $R_S$ .

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (6)$$

$K_1$  is set to 0.5

When over current operation or short circuit operation happens, the output current will be limited at  $I_{OUT-LIM}$ . The V-I curve is shown as Fig.6.

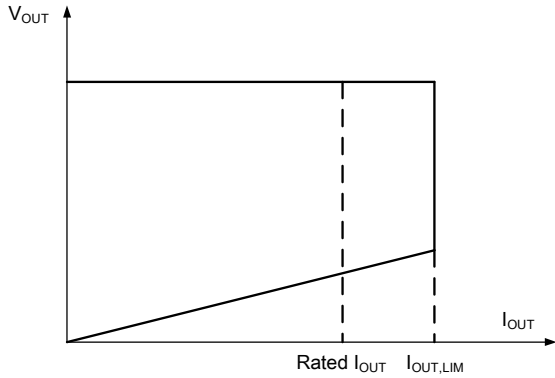


Fig. 6 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage  $\Delta V_{ISEN-C}$  is added to ISEN pin during ON time to improve such performance. This  $\Delta V_{ISEN-C}$  is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN-C} = V_{BUS} \times \frac{N_{AUX}}{N_p} \times \frac{1}{R_{VSENU}} \times k_2 \quad (7)$$

Where  $R_{VSENU}$  is the upper resistor of the divider;  $k_2$  is an internal constant as the modification coefficient.

The compensation is mainly related with  $R_{VSENU}$ , larger compensation is achieved with smaller  $R_{VSENU}$ . Normally,  $R_{VSENU}$  ranges from 50k $\Omega$ ~150k $\Omega$ .

### Cable Compensation

SY5002C has cable compensation to regulate the output voltage for better load regulation at cable terminal. When the converter output load increases from no load to full load, the voltage drops on the output cable are compensated by decreasing the voltage feedback signals, which is shown by Fig. 7.

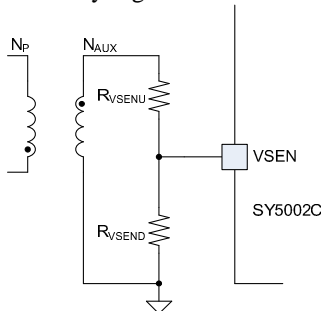


Fig. 7 Cable Compensation

$$R_{Cable} = 2k_3 \cdot R_S \cdot \frac{N_S}{N_p} \cdot R_{VSENU} \cdot \frac{N_S}{N_{AUX}} \quad (8)$$

$k_3$  is set to 17.5 $\mu$ A/V

$R_{Cable}$  is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of  $R_{VSENU}$  to achieve good load regulation of different output cables. The larger  $R_{VSENU}$ , the stronger cable compensation effect will be achieved.

If the output current is below 10% the OCP point, there is no cable compensation.

### Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN.

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases, the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when  $V_{VIN}$  below  $V_{VIN-OFF}$  within 64 times.

When the output voltage is not low enough to disable valley detection in short condition, SY5002C will operate in CC mode until  $V_{IN}$  is below  $V_{IN-OFF}$ .

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor  $R_{AUX}$  is needed.

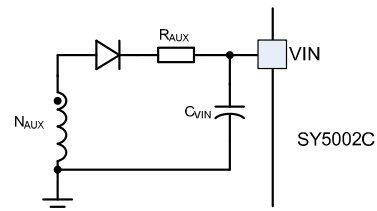


Fig. 8 Filter resistor  $R_{AUX}$

### Output voltage OVP protection

The secondary maximum voltage is limited by the SY5002C. When the VSEN pin signal exceeds 1.45V, SY5002C will stop switching and discharge the VIN



voltage. Once  $V_{VIN}$  is below  $V_{VIN-OFF}$ , the IC will shut down and be charged again by HV start up.

### VSEN pin short protection

The SY5002C has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VIN voltage. Once  $V_{VIN}$  is below  $V_{VIN-OFF}$ , the IC will shut down and be charged again by HV start up. In order to ensure reliable detection, the pull-down resistor should larger than 2kΩ.

## Power Device Design

### MOSFET and DIODE

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (8)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (9)$$

Where  $V_{AC\_MAX}$  is maximum input AC RMS voltage;  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the rated output voltage;  $V_{D\_F}$  is the forward voltage of secondary power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (10)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (11)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (12)$$

$$I_{D\_AVG} = I_{OUT} \quad (13)$$

Where  $I_{P\_PK\_MAX}$  and  $I_{P\_RMS\_MAX}$  are maximum primary peak current and RMS current, which will be introduced later.

### Transformer ( $N_{PS}$ and $L_M$ )

$N_{PS}$  is limited by the electrical stress of the power MOSFET:

$$N_{PS} \leq \frac{V_{MOS\_BR\_DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (14)$$

Where  $V_{MOS\_BR\_DS}$  is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle  $t_s$  consists of three parts: current rising time  $t_1$ , current falling time  $t_2$  and quasi-resonant time  $t_3$  shown in Fig.9.

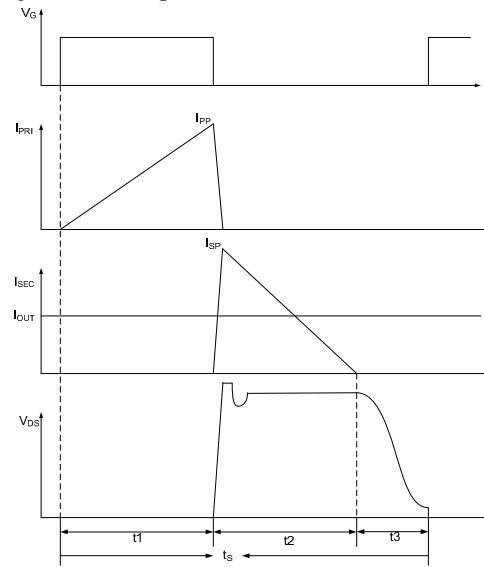


Fig.9 switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency  $f_{S\_MIN}$  is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select  $N_{PS}$

$$N_{PS} \leq \frac{V_{MOS\_BR\_DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (15)$$

(b) Preset minimum frequency  $f_{S\_MIN}$

(c) Compute inductor  $L_M$  and maximum primary peak current  $I_{P\_PK\_MAX}$



$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (16)$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (17)$$

Where  $C_{Drain}$  is the parasitic capacitance at drain of MOSFET;  $\eta$  is the efficiency;  $P_{OUT}$  is rated full load power

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_m \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (18)$$

$$t_2 = \frac{L_m \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (19)$$

$$t_s = \frac{1}{f_{S\_MIN}} \quad (20)$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} \quad (21)$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (22)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P\_PK\_MAX} \cdot \sqrt{\frac{t_2}{t_s}} \quad (23)$$

### Transformer design ( $N_p, N_s, N_{AUX}$ )

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	$N_{PS}$
Inductance	$L_m$
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area  $A_e$ .

(b) Preset the maximum magnetic flux  $\Delta B$

$$\Delta B = 0.22 \sim 0.26 T$$

(c) Compute primary turn  $N_p$

$$N_p = \frac{L_m \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (24)$$

(d) Compute secondary turn  $N_s$

$$N_s = \frac{N_p}{N_{PS}} \quad (25)$$

(e) compute auxiliary turn  $N_{AUX}$

$$N_{AUX} = N_s \times \frac{V_{VIN}}{V_{OUT}} \quad (26)$$

Where  $V_{VIN}$  is the working voltage of VIN pin (11V~15V is recommended).

(f) Select an appropriate wire diameter

With  $I_{P\_RMS\_MAX}$  and  $I_{S\_RMS\_MAX}$ , select appropriate wire to make sure the current density ranges from 4A/mm<sup>2</sup> to 10A/mm<sup>2</sup>.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

### Input capacitor $C_{BUS}$

Generally, the input capacitor  $C_{BUS}$  is selected by

$$C_{BUS} = 2 \sim 3 \mu F / W$$

Or more accurately by

$$C_{BUS} = \frac{\arcsin\left(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}}\right) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN} V_{AC\_MIN}^2 \left[1 - \left(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}}\right)^2\right]} \quad (27)$$

Where  $\Delta V_{BUS}$  is the voltage ripple of BUS line.

### RCD snubber for MOSFET

The power loss of the snubber  $P_{RCD}$  is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_s}{\Delta V_s} \times \frac{L_K}{L_M} \times P_{OUT} \quad (28)$$

Where  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the output voltage;  $V_{D-F}$  is the forward voltage of the power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber;  $L_K$  is the leakage inductor;  $L_M$  is the inductance of the Flyback transformer;  $P_{OUT}$  is the output power.

The  $R_{RCD}$  is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D-F}) + \Delta V_S)^2}{P_{RCD}} \quad (29)$$

The  $C_{RCD}$  is related with the voltage ripple of the snubber  $\Delta V_{C-RCD}$ :

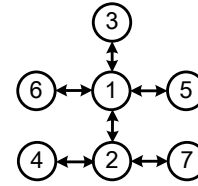
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D-F}) + \Delta V_S}{R_{RCD} f_s \Delta V_{C-RCD}} \quad (30)$$

## Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

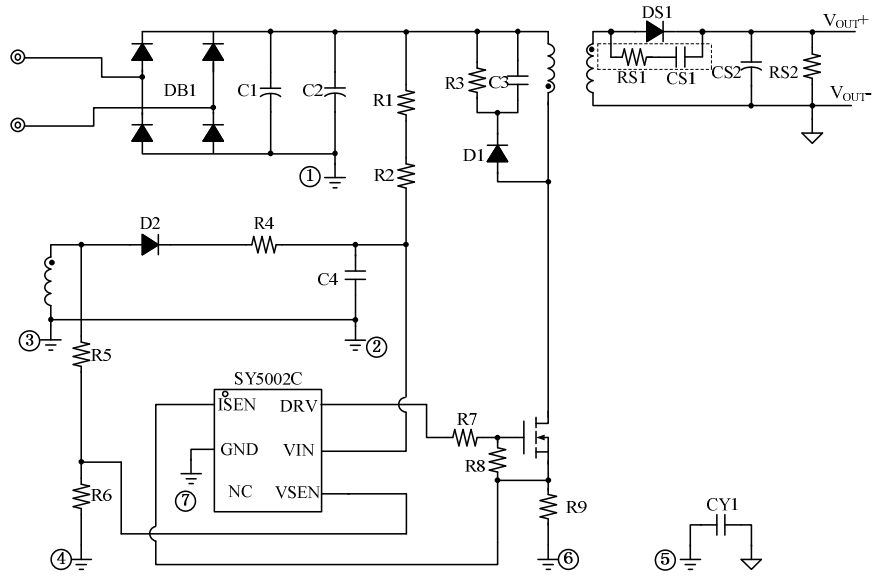


Ground ①: ground of BUS line capacitor  
 Ground ②: ground of bias supply capacitor  
 Ground ③: ground node of auxiliary winding  
 Ground ④: ground node of divider resistor  
 Ground ⑤: primary ground node of Y capacitor  
 Ground ⑥: ground node of current sample resistor.  
 Ground ⑦: ground of IC GND.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.



Note : Ground node of current sample resistor must be connected to the ground of bus line capacitor



## Design Notice

1. At no load, secondary side diode freewheeling time should be more than 1.8us.
2. VIN voltage prefer to larger than 11V for all conditions.
3. Some transformers structure may induce larger spike or larger ring on the current sample resistor at the initial of the primary switch turning on. This spike or ring may cause wrongly detection of the peak current and make the switch turn off earlier, so the accuracy feedback voltage sample cannot be guaranteed. The recommend structures are: 0.5Pri.----shielding----Sec.----Aux.----0.5Pri.or Pri.----shielding----Sec.----Aux.; Do not use the structure like 0.5Pri.----Aux.----Sec.----Shielding.----0.5Pri..
4. RCD snubber's influence:  
At no load and light load, capacitor's voltage may be discharged to a small value, when primary switch turn off , peak current needs to charge the snubber capacitor, this will affect the feedback voltage sample and include larger ripple or other issues. The recommend parameters is: When  $I_{min}(I_{min}=0.15V/R_s)$  is 0.1A, the snubber capacitor should not larger than 470pF.
5. At heavy load, the peak-to-peak voltage at the VSEN pin should be less than approximately 100mV<sub>p-p</sub> after off-min time(1.8us). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
6.  $R_{VSENU}$  is the upper resistor of the divider .Normally, its value should be in 50kΩ~150kΩ.

## Design Example

A design example of typical application is shown below step by step.

### #1. Identify design specification

Design Specification			
V <sub>AC</sub> (RMS)	90V~264V	V <sub>OUT</sub>	12V
I <sub>OUT</sub>	2A	η	90%

### #2. Transformer design (N<sub>PS</sub>, L<sub>M</sub>)

Refer to Power Device Design

Conditions			
V <sub>AC-MIN</sub>	90V	V <sub>AC-MAX</sub>	264V
ΔV <sub>S</sub>	75V	V <sub>MOS-(BR)DS</sub>	600V
P <sub>OUT</sub> (max)	24W	V <sub>D,F</sub>	1V
C <sub>Drain</sub>	100pF	f <sub>S-MIN</sub>	60kHz
ΔV <sub>BUS</sub>	30% V <sub>BUS</sub>		

#### (a) Compute turns ratio N<sub>PS</sub> first

$$\begin{aligned}
 N_{PS} &\leq \frac{V_{MOS-(BR)DS} \times 90\% - \sqrt{2}V_{AC-MAX} - \Delta V_S}{V_{OUT} + V_{D,F}} \\
 &= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 75V}{12V + 1V} \\
 &= 7.05
 \end{aligned}$$

N<sub>PS</sub> is set to

$$N_{PS} = 7$$

#### (b) f<sub>S,MIN</sub> is preset

$$f_{S,MIN} = 60kHz$$

#### (c) Compute inductor L<sub>M</sub> and maximum primary peak current I<sub>P,PK,MAX</sub>

$$\begin{aligned}
 I_{P\_PK\_MAX} &= \frac{2P_{OUT}}{\eta \times (\sqrt{2}V_{AC-MIN} - \Delta V_{BUS})} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \\
 &= \frac{2 \times 24W}{0.9 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 24W}{0.9 \times 7 \times (12V + 1V)} + \pi \times \sqrt{\frac{2 \times 24W}{0.9} \times 100pF \times 60KHz} \\
 &= 1.241A \\
 L_m &= \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \\
 &= \frac{2 \times 24W}{0.9 \times (1.241A)^2 \times 60KHz} \\
 &= 0.577mH
 \end{aligned}$$



Set:  $L_m=0.55\text{mH}$

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} = \frac{0.55\text{mH} \times 1.241\text{A}}{\sqrt{2} \times 90\text{V}} = 5.36\mu\text{s}$$

$$t_2 = \frac{L_m \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{0.55\text{mH} \times 1.241\text{A}}{7 \times (12\text{V} + 1\text{V})} = 7.5\mu\text{s}$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{0.55\text{mH} \times 100\text{pF}} = 0.737\mu\text{s}$$

$$t_s = t_1 + t_2 + t_3 = 5.36\mu\text{s} + 7.5\mu\text{s} + 0.737\mu\text{s} = 13.6\mu\text{s}$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} = \frac{\sqrt{3}}{3} \times 1.241\text{A} \times \sqrt{\frac{5.36\mu\text{s}}{13.6\mu\text{s}}} = 0.45\text{A}$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 7 \times 1.241\text{A} = 8.686\text{A}$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_s}} = 7 \times \frac{\sqrt{3}}{3} \times 1.241\text{A} \times \sqrt{\frac{7.5\mu\text{s}}{13.6\mu\text{s}}} = 3.724\text{A}$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
$V_{AC\_MAX}$	264V	$N_{PS}$	7
$V_{OUT}$	12V	$V_{D\_F}$	1V
$\Delta V_S$	75V		

(a) Compute the voltage and the current stress of MOSFET:

$$\begin{aligned} V_{MOS\_DS\_MAX} &= \sqrt{2} V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \\ &= \sqrt{2} \times 264\text{V} + 7 \times (12\text{V} + 1\text{V}) + 75\text{V} \\ &= 539\text{V} \end{aligned}$$

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 1.241\text{A}$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.45\text{A}$$

(b) Compute the voltage and the current stress of secondary power diode

$$V_{D,R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$

$$= \frac{\sqrt{2} \times 264V}{7} + 12V$$

$$= 65.3V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 7 \times 1.241A = 8.686A$$

$$I_{D\_AVG} = 2A$$

#4. Select the input capacitor  $C_{IN}$

Refer to input capacitor  $C_{IN}$  Design

Known conditions at this step			
$V_{AC\_MIN}$	90V	$\Delta V_{BUS}$	30% $V_{AC\_MIN}$

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN} V_{AC\_MIN}^2 [1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$= \frac{\arcsin(1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V}) + \frac{\pi}{2}}{\pi} \times \frac{24W}{0.9} \times \frac{1}{2 \times 50Hz \times 90V^2 \times [1 - (1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V})^2]}$$

$$= 48.2\mu F$$

Set  $C_{BUS}$

$$C_{BUS} = 44\mu F$$

Where  $\Delta V_{BUS}$  is the voltage ripple of BUS line.

#5. Set VIN pin

Refer to Start up

Conditions			
$V_{BUS\_MIN}$	$90V \times \sqrt{2}$	$V_{BUS\_MAX}$	$264V \times \sqrt{2}$
$I_{ST}$	4 $\mu A$ (typical)	$V_{IN\_ON}$	14.7V (typical)
$I_{VIN\_OVP}$	7.5mA (typical)	$t_{ST}$	2s (designed by user)

(a)  $R_{ST}$  is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{90V \times 1.414}{4\mu A} = 31.81M\Omega,$$





$$R_{ST} > \frac{V_{BUS}}{I_{VIN\_OVP}} = \frac{264V \times 1.414}{7.5mA} = 49.77k\Omega$$

Set  $R_{ST}$

$$R_{ST} = 4M$$

(b) Design  $C_{VIN}$

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} = \frac{(\frac{90V \times 1.414}{6M\Omega} - 4\mu A) \times 2s}{14.7V} = 2.34\mu F$$

Set  $C_{VIN}$

$$C_{VIN} = 3.3\mu F$$

#6. Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
$k_1$	0.5	$N_{PS}$	7
$V_{REF}$	0.42V	$I_{OUT\_LIM}$	2.4A

The current sense resistor is

$$R_s = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} = \frac{0.5 \times 0.42V \times 7}{2.4A} = 0.613\Omega$$

Set  $R_s$

$$R_s = 0.556\Omega$$

#7. Set  $V_{SEN}$  pin

Refer to  $V_{OUT}$

First compute  $R_{VSENU}$

Conditions			
$V_{OUT}$	12V	$V_{VSEN\_REF}$	1.25V
$R_{Cable}$	0.2 $\Omega$	$N_s$	13
$N_{AUX}$	15	$K_3$	17.5uA/V

$$R_{VSENU} = \frac{N_p}{N_s} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_s} \cdot \frac{1}{2K_3 \cdot R_s} = 83K\Omega$$



Set  $R_{VSEN_U}$

$$R_{VSEN_U} = 82k\Omega$$

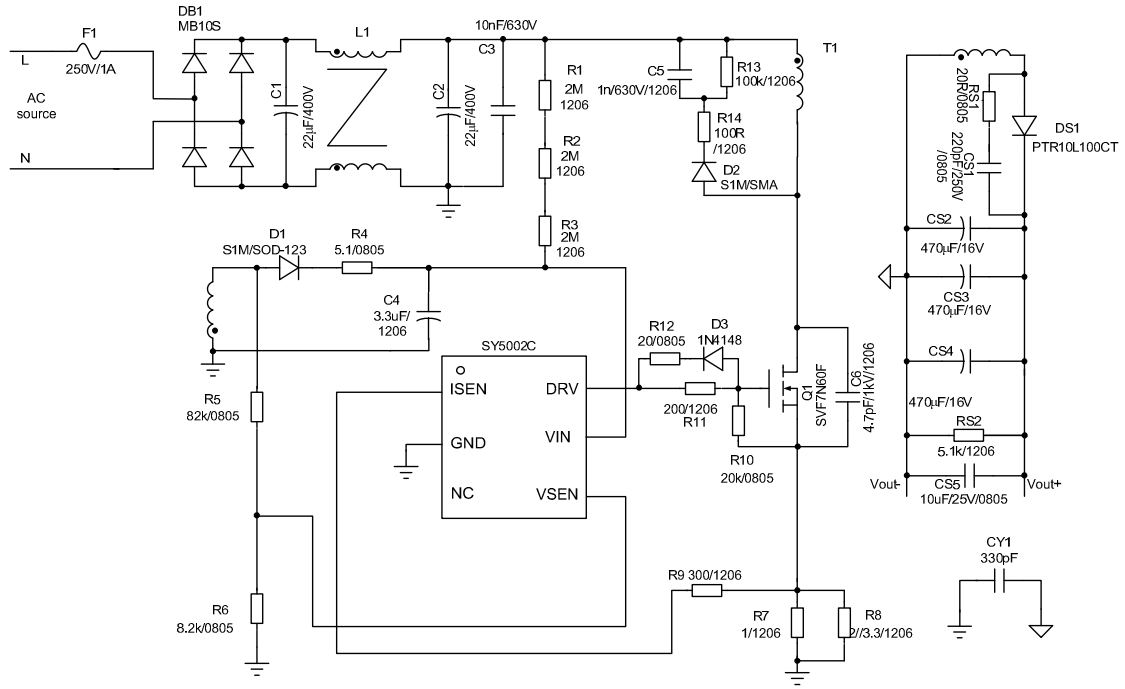
Then compute  $R_{VSEN_D}$

$$R_{VSEN_D} = \frac{R_{VSEN_U}}{\frac{V_{OUT} N_{AUX}}{V_{VSEN\_REF} N_S} - 1} = \frac{100K}{\left(\frac{12V \times 15}{1.25V \times 13} - 1\right)} = 8.14K$$

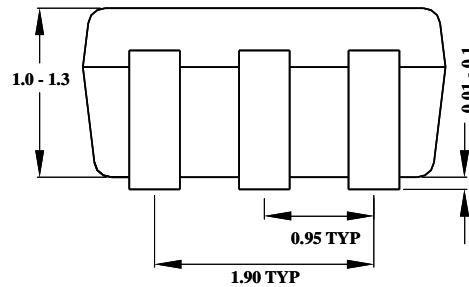
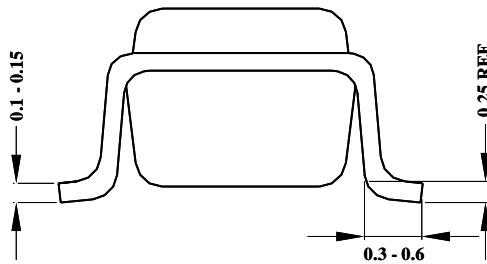
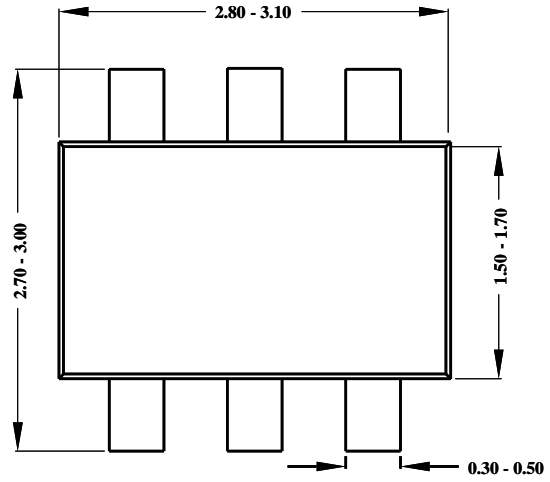
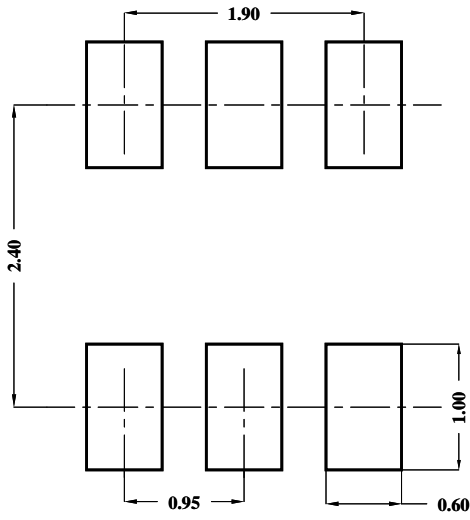
$$R_{VSEN_D} = 8.2k\Omega$$



## #8. Final result



**SOT23-6 Package outline & PCB layout design**

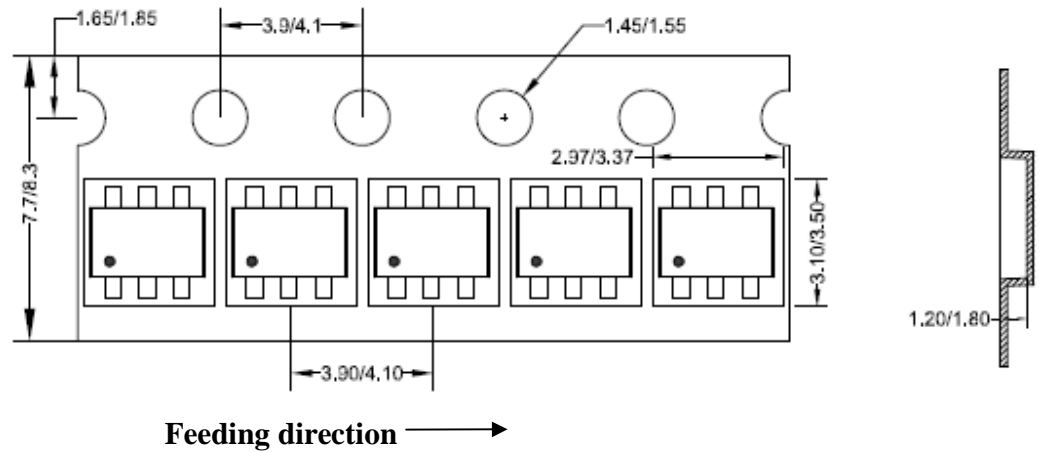


**Notes:** All dimensions are in millimeters.  
 All dimensions don't include mold flash & metal burr.

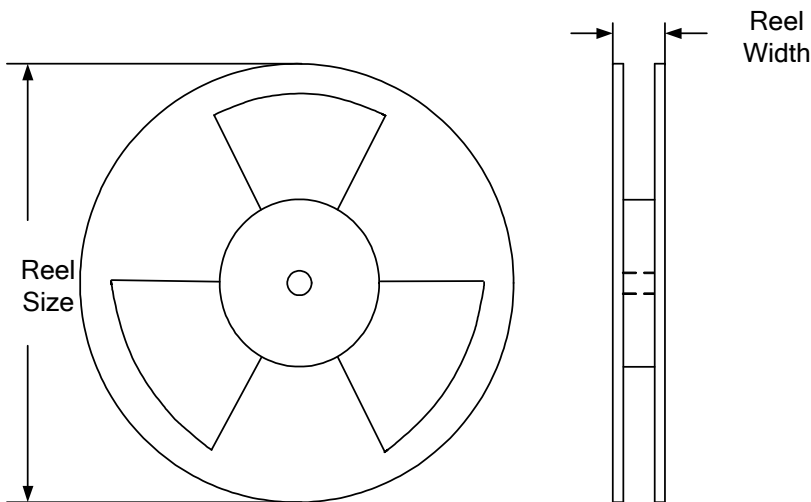
**Taping & Reel Specification**

**1. Taping orientation**

SOT23-6



**2. Carrier Tape & Reel specification for packages**



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	8.4	280	160	3000

**3. Others: NA**