



# Application Note: AN\_SY7065/SY7065A

## 1.8V Minimum Input and 5.5V Maximum Output 5A Peak Current Synchronous Boost with Output Disconnect

### General Description

SY7065/SY7065A is a high efficiency synchronous boost regulator that converts down to 1.8V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

### Ordering Information

SY7065 □(□□)□  
 □ Temperature Code  
 □ Package Code  
 □ Optional Spec Code

Temperature Range: -40°C to 85°C

| Ordering Number | Package type | Note |
|-----------------|--------------|------|
| SY7065QMC       | QFN2X2-10    | ---- |
| SY7065AQMC      | QFN2X2-10    | ---- |

### Features

- 1.8V Minimum input voltage
- Adjustable output voltage from 2.5V to 5.5V
- 5A peak current limit
- Input under voltage lockout
- Load disconnect during shutdown
- Output over voltage protection
- Input battery voltage monitor
- Automatic output discharge at shutdown:
  - o SY7065: Auto output discharge function
  - o SY7065A: No output discharge function
- Low  $R_{DS(ON)}$  (main switch/synchronous switch) at 5.0V output: 20/40mΩ
- Compact package: QFN2x2-10

### Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

### Typical Applications

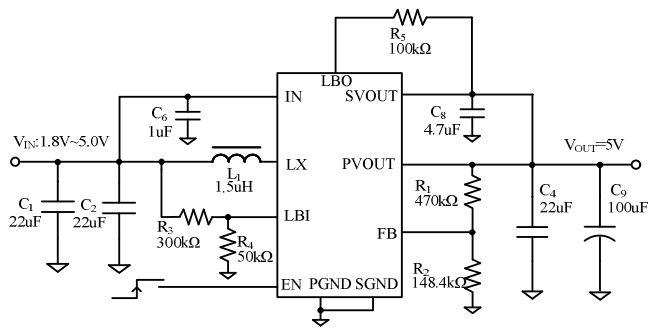


Figure 1. Schematic Diagram

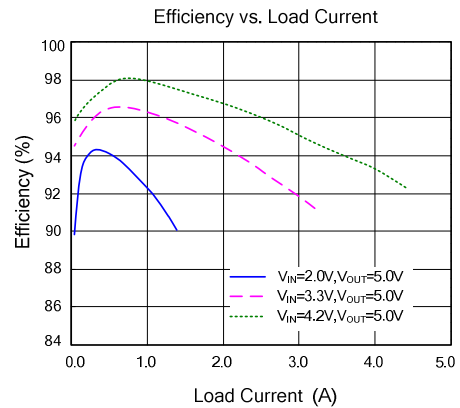
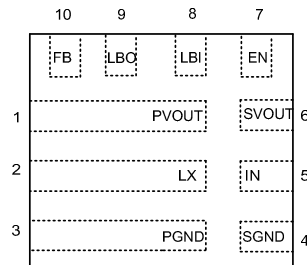


Figure 2. Efficiency Figure



# AN\_SY7065/SY7065A

## Pinout (top view)



(QFN2X2-10)

Top mark: **RCxyz** for **SY7065** (Device code: RC., x=year code, y=week code, z=lot number code)  
**VLxyz** for **SY7065A** (Device code: VL., x=year code, y=week code, z=lot number code)

| Name  | QFN2X2-10 | Description  |
|-------|-----------|--|
| PVOUT | 1         | Power output pin. Decouple this pin to GND pin with at least 22uF ceramic cap.   |
| SVOUT | 6         | Signal output pin. Decouple this pin to GND pin with at least 4.7uF ceramic cap for noise immunity consideration.  |
| LX    | 2         | Inductor node. Connect an inductor between IN pin and LX pin.  |
| PGND  | 3         | Power ground pin.  |
| SGND  | 4         | Signal ground pin.   |
| IN    | 5         | Signal input pin.  |
| EN    | 7         | Enable pin. Internal integrated with 1Mohm pull down resistor.   |
| LBI   | 8         | Low battery comparator input.  |
| FB    | 10        | Feedback pin. Connect a resistor R1 between OUT and FB, and a resistor R2 between FB and GND to program the output voltage. $V_{OUT}=1.2V*(R_1/R_2+1)$ . |
| LBO   | 9         | Low battery comparator output.(open drain) .   |

## Absolute Maximum Ratings (Note 1)

|  |       |                |
|--|-------|----------------|
| EN   | ----- | $V_{OUT}+0.3V$ |
| Other Pins   | ----- | 6V             |
| Power Dissipation, $P_D@ T_A=25^\circ C$ QFN2x2-10 | ----- | 2.5W           |
| Package Thermal Resistance (Note 2)                |       |                |
| $\theta_{JA}$                                      | ----- | 50°C/W         |
| $\theta_{JC}$                                      | ----- | 10°C/W         |
| Junction Temperature Range                         | ----- | 150°C          |
| Lead Temperature (Soldering, 10 sec.)              | ----- | 260°C          |
| Storage Temperature Range                          | ----- | -65°C to 150°C |

## Recommended Operating Conditions (Note 3)

|                            |       |                      |
|----------------------------|-------|----------------------|
| IN                         | ----- | 1.8V to 5.25V        |
| PVOUT, SVOUT               | ----- | 2.5V to 5.5V         |
| EN                         | ----- | 0V to $V_{OUT}+0.3V$ |
| All other pins             | ----- | 0-5.5V               |
| Junction Temperature Range | ----- | -40°C to 125°C       |
| Ambient Temperature Range  | ----- | -40°C to 85°C        |



## AN\_SY7065/SY7065A

### Electrical Characteristics

( $V_{IN}=2.4V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=500mA$ ,  $T_A=25^{\circ}C$  unless otherwise specified)

| Parameter                      | Symbol         | Test Conditions                            | Min   | Typ | Max   | Unit        |
|--------------------------------|----------------|--|-------|-----|-------|-------------|
| Input Voltage                  | $V_{IN}$       |  | 1.8   |     | 5.25  | V           |
| Output Voltage Range           | $V_{OUT}$      |  | 2.5   |     | 5.5   | V           |
| Quiescent Current              | $V_{IN}$       | $I_o=0A, V_{EN}=V_{IN}=1.8V, V_{OUT}=5.0V$ |       | 10  |       | $\mu A$     |
|                                | $V_{OUT}$      |  |       | 27  |       | $\mu A$     |
| Shutdown Current               | $I_{SHDN}$     | $V_{EN}=0V, V_{IN}=2.4V$                   |       | 0.1 | 1     | $\mu A$     |
| Linear charge current          | $I_{CHARGE}$   | $V_{OUT} \leq 1V$                          |       | 1.2 |       | A           |
|                                |                | $1V < V_{OUT} < 90\%V_{IN}$                |       | 1.0 |       |             |
| Soft-start time                | $T_{SS}$       |  |       | 1   |       | ms          |
| Input Vin UVLO threshold       | $V_{UVLO}$     |  |       |     | 1.78  | V           |
| Vin UVLO hysteresis            | $V_{HYS}$      |  |       | 0.1 |       | V           |
| EN Rising Threshold            | $V_{ENH}$      |  | 1.2   |     |       | V           |
| EN Falling Threshold           | $V_{ENL}$      |  |       |     | 0.4   | V           |
| LBI Voltage Threshold          | $V_{LBI}$      |  | 1.176 | 1.2 | 1.224 | V           |
| LBI Input Hysteresis           | $V_{LBI\_HYS}$ |  |       | 20  |       | mV          |
| Low Side Main FET $R_{ON}$     | $R_{DS(ON)1}$  | $V_{OUT}=5.0V$                             |       | 20  |       | $m\Omega$   |
| Synchronous FET $R_{ON}$       | $R_{DS(ON)2}$  | $V_{OUT}=5.0V$                             |       | 40  |       | $m\Omega$   |
| Main FET Current Limit         | $I_{LIM1}$     |  | 5.0   |     |       | A           |
| Switching Frequency            | $f_{SW}$       |  |       | 500 |       | kHz         |
| Feedback Reference Voltage     | $V_{REF}$      |  | 1.182 | 1.2 | 1.218 | V           |
| Output over voltage protection | $V_{OVP}$      |  |       | 6   |       | V           |
| Minimum on time                | $T_{ON\_MIN}$  |  |       | 100 |       | ns          |
| Minimum off time               | $T_{OFF\_MIN}$ |  |       | 100 |       | ns          |
| Max on time                    | $T_{ON\_MAX}$  |  |       | 2   |       | $\mu s$     |
| Thermal Shutdown Temperature   | $T_{SD}$       |  |       | 150 |       | $^{\circ}C$ |
| Thermal Shutdown hysteresis    | $T_{HYS}$      |  |       | 20  |       | $^{\circ}C$ |
| Output Discharge Resistor      | $R_{DSC}$      |  |       | 80  |       | $\Omega$    |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

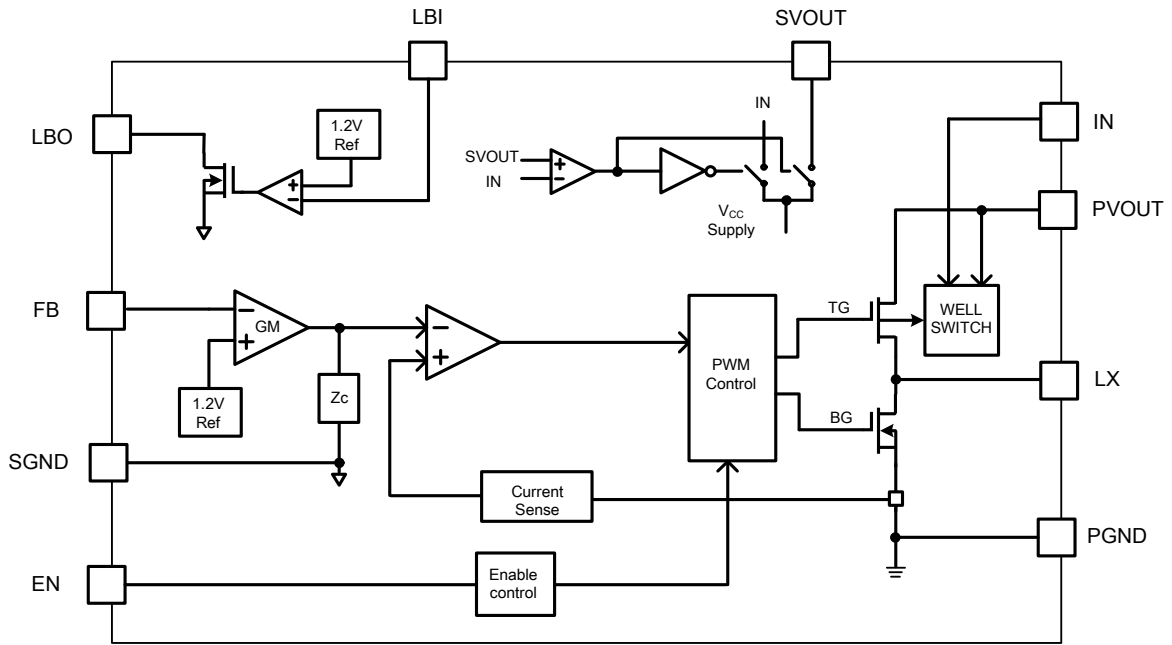
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^{\circ}C$  on a four-layer Silergy Evaluation Board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.



# AN\_SY7065/SY7065A

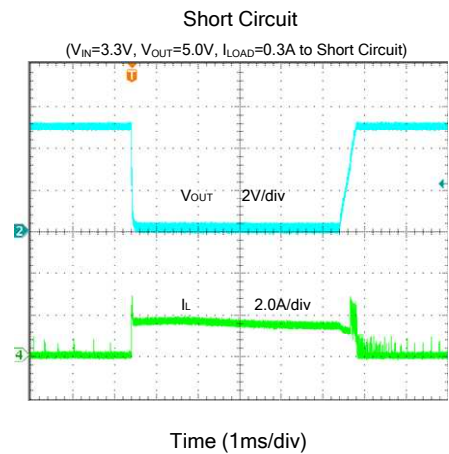
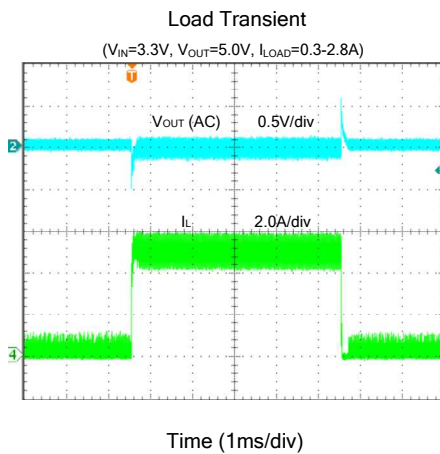
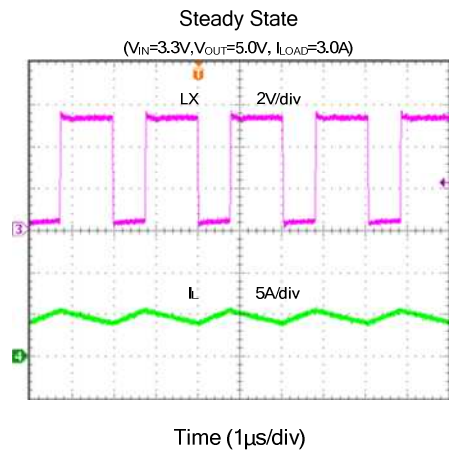
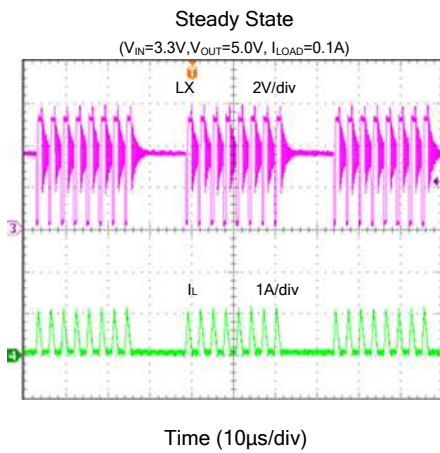
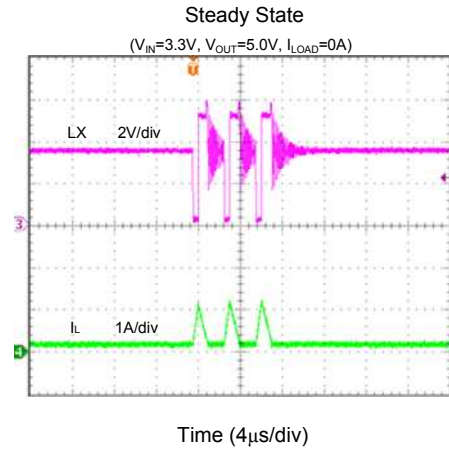
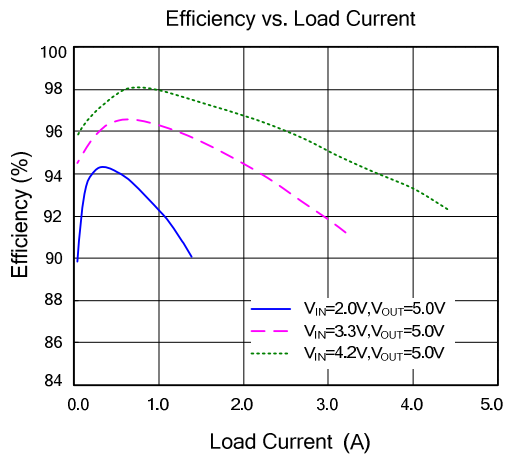
## Block Diagram





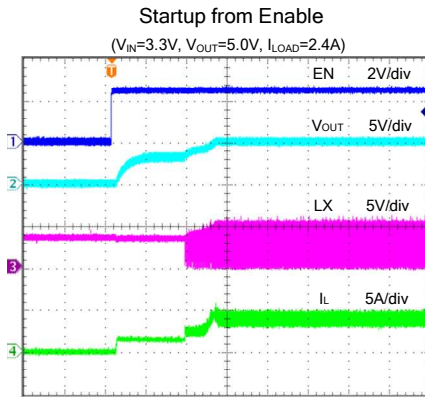
# AN\_SY7065/SY7065A

## Typical Performance Characteristics (for SY7065)

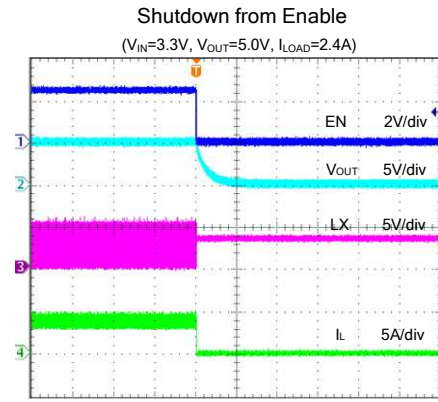




# AN\_SY7065/SY7065A



Time (1ms/div)



Time (1ms/div)

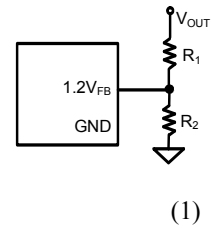
## Applications Information

Because of the high integration for SY7065/A, only input capacitor  $C_{IN}$ , output capacitor  $C_{OUT}$ , inductor  $L$  and feedback resistors ( $R_1$  and  $R_2$ ) need to be selected for the targeted applications specifications.

### Feedback resistor dividers $R_1$ and $R_2$ :

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ . A value of between  $10k\Omega$  and  $1M\Omega$  is recommended for both resistors. If  $V_{OUT}$  is  $5.0V$ ,  $R_1=470k\Omega$  is chosen, using following equation, then  $R_2$  can be calculated to be  $148.4k\Omega$ :

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1$$



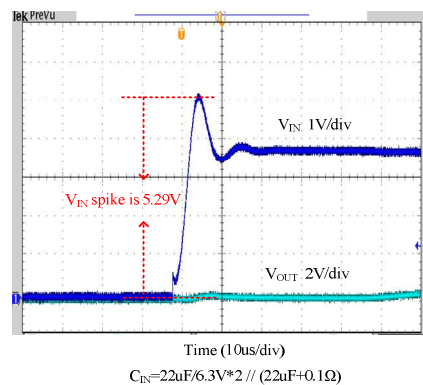
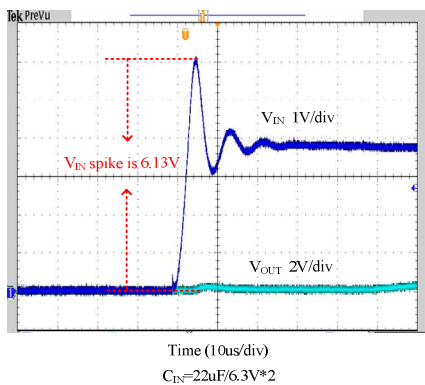
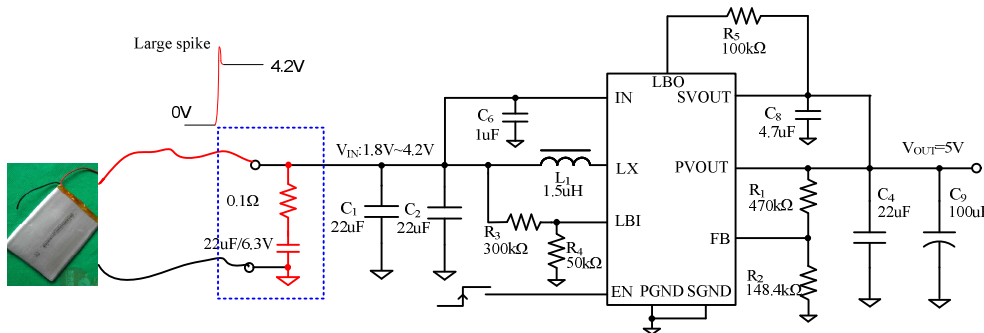
### Input capacitor $C_{IN}$ :

The input capacitor is selected to handle the input ripple current requirements. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with  $6.3V$  rating and greater than  $22\mu F$  capacitance.

### Li-Ion battery hot plug consideration:

In the mass production stage, the Li-Ion Battery will always hot plug in between IC IN and GND pin. The hot plug may lead to large voltage spike and even lead to IC EOS fail. To avoid this potential risk, 1pcs  $22\mu F$  ceramic cap serial with  $0.1\Omega$  resistor is recommended to absorb the input voltage spike.

With the recommended input absorb solution, the voltage spike can be reduced from  $6.13V$  to  $5.29V$ .





### Inductor L Selection:

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%} \quad (2)$$

where  $F_{SW}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current. The SY7065/A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

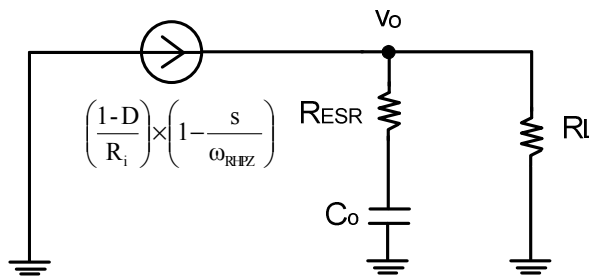
$$I_{SAT,MIN} > \left( \frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L} \quad (3)$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 50\text{mohm}$  to achieve a good overall efficiency.

### Inductor Vs. Output Capacitor:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Care should be taken to minimize the loop area formed by  $C_{OUT}$ , and OUT/GND pins. It's recommended to use a X5R or better grade ceramic capacitor with 10V rating and great than 22uF capacitance to decouple the high frequency current. And also a tantalum capacitor with 16V rating and great than 100uF capacitance is recommended for the stability consideration.

All continuous mode boost converters have a right half plane zero (RHPZ) due to the inductor being removed from the output during charging. In a converter with current mode control, inner current feedback loop allows the switch, inductor and modulator to be lumped together into a small signal variable current source, shown as follow.



the power stage approximate transfer function is:

$$G_c(s) = \frac{(1-D) \times R_L}{R_i} \times \frac{\left( 1 + \frac{s}{\omega_{ESR}} \right) \left( 1 - \frac{s}{\omega_{RHPZ}} \right)}{1 + \frac{s}{\omega_p}} \quad (4)$$





## AN\_SY7065/SY7065A

Where

$$\omega_{\text{ESR}} = \frac{1}{R_{\text{ESR}} C_{\text{O}}} \quad (5)$$

$$\omega_{\text{p}} = \frac{1}{(R_{\text{ESR}} + R_{\text{L}}) \times C_{\text{O}}} \quad (6)$$

$$\omega_{\text{RHPZ}} = \frac{R_{\text{L}}}{L} \times \left( \frac{V_{\text{IN}}}{V_{\text{OUT}}} \right)^2 \quad (7)$$

As the equation 4 shows, Boost convert with current mode control transfer function is consist of one ESR zero, one right half plane zero and one pole. Right half plane zero brings 20dB/decade gain increase, 90 degrees phase drop. So the bandwidth of boost converter MUST be lower than  $f_{\text{RHPZ}}$ .

As shown in equation 7, right half plane zero is depend on  $R_{\text{L}}$ ,  $L$  and duty cycle. Larger inductor lead to lower  $f_{\text{RHPZ}}$ , so bandwidth should be designed lower than  $f_{\text{RHPZ}}$ .

Some low profile application may prefer to use the ceramic capacitor solution and some low cost application may use the Electrolytic cap to reduce the BOM cost.

Below is selection table based on different inductance and output capacitor.

**Inductance Vs. Output Capacitor Selection Table**

| Inductance    |       | Low profile capacitor application |                       | Low cost capacitor application |
|---------------|-------|-----------------------------------|-----------------------|--------------------------------|
| Part Number   | L(uH) | Part Number                       | $C_{\text{OUT}}$ (uF) | $C_{\text{OUT}}$ (uF)          |
| SPM6530T-1R0M | 1.0   | C3216X5R1A226M                    | 22uF/10V×3pcs         | 22uF/10V+100uF(E-cap)          |
| SPM6530T-1R5M | 1.5   | C3216X5R1A226M                    | 22uF/10V×4pcs         | 22uF/10V+100uF(E-cap)          |
| SPM6530T-2R2M | 2.2   | C3216X5R1A226M                    | 22uF/10V×5pcs         | 22uF/10V+200uF(E-cap)          |

### Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY7065/A shutdown current drops to lower than 1uA, driving the EN pin high (> 1.2V) will turn on the IC again.

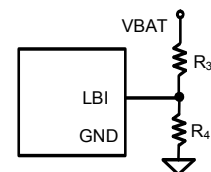
### Low Battery Detector Function-LBI/LBO

The low-battery detector function is used to monitor the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage.

The function is active only when the device is enabled. When the device is disabled, LBO stays at high impedance. The detection threshold is 1.2V at LBI. During normal operation, LBO stays at high impedance when the voltage applied at LBI is above the threshold. It is active low when the voltage at LBI goes below 1.2V.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to LBI pin. The resistive divider scales down the battery voltage to a voltage level of 1.2V, which is then compared to LBI threshold voltage. The LBI pin has a built-in hysteresis of 20mV. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

$R_3$  and  $R_4$  are designed to program the proper low battery threshold voltage. The voltage across  $R_4$  is equal to the LBI voltage threshold that is generated on-chip, which has a value of 1.2V. The value of resistor  $R_3$ , depending on the desired minimum battery voltage VBAT, can be calculated as:



$$R_3 = \frac{V_{BAT} - 1.2V}{1.2V} R_4 \quad (9)$$

The output of the low battery monitor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pull up resistor with a recommended value of 100kΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the DC/DC converter. If not used, the LBO pin can be left floating or tied to GND.

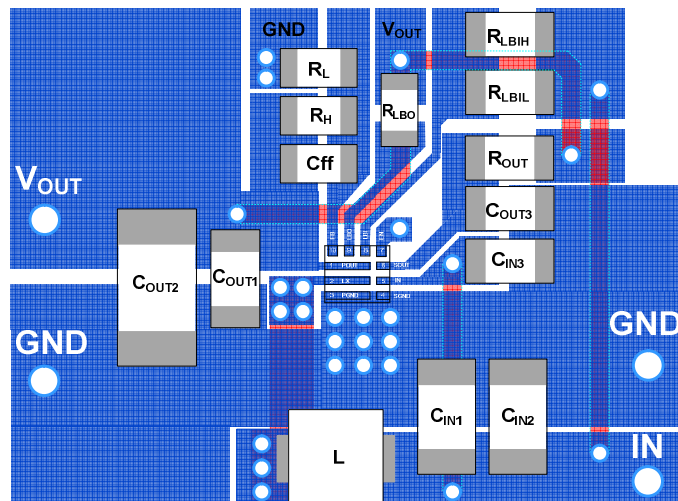
### Layout Design Consideration:

For the best efficiency and minimum noise problems, we should place the following components close to the IC: C<sub>IN</sub>, C<sub>OUT</sub>, L, R<sub>1</sub> and R<sub>2</sub>.

- 1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly recommended.
- 2) C<sub>OUT</sub> must be close with Pins PVOUT and PGND. The loop area formed by C<sub>OUT</sub> and GND must be minimized.
- 3) To minimize the output decouple loop area, LX trace is recommended to be routed on bottom or middle layer through via.
- 4) SVOUT is the power supply pin for the internal control circuit. Don't connect to PVOUT pin directly. A 4.7uF ceramic cap is strongly recommended to decouple SVOUT pin to SGND pin. Please use a jump wire to connect SVOUT pin to output capacitor side.
- 5) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 6) The components R<sub>1</sub> and R<sub>2</sub>, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

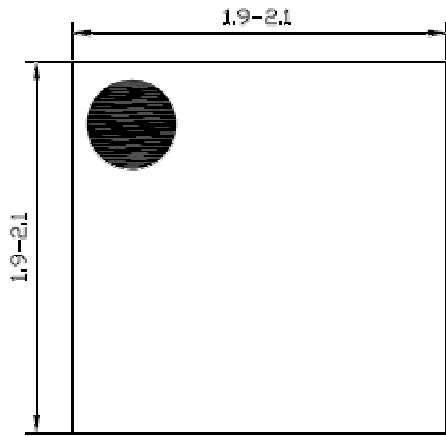
### PCB Layout Suggestion

| FB | LBO   | LBI | EN |       |
|----|-------|-----|----|-------|
| 10 | 9     | 8   | 7  |       |
| 1  | PVOUT |     | 6  | SVOUT |
| 2  | LX    |     | 5  | IN    |
| 3  | PGND  |     | 4  | SGND  |

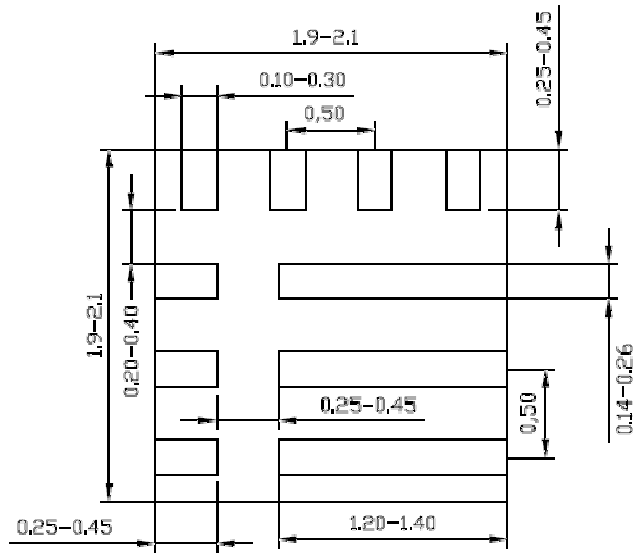




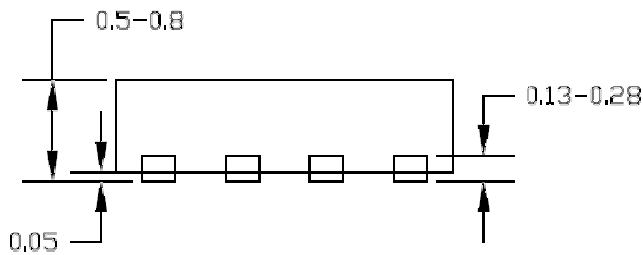
**QFN2x2-10L FC Package Outline**



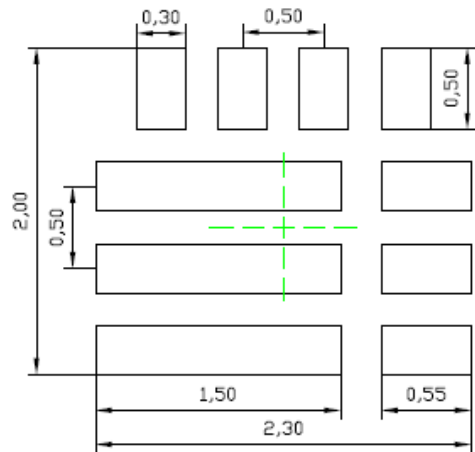
**Top View**



**Bottom View**



**Side View**



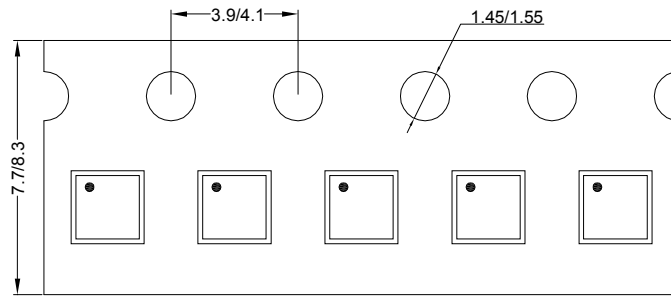
**Recommended PCB Layout  
(Reference only)**

**Notes:** All dimension in MM and exclude mold flash & metal burr.

## Taping & Reel Specification

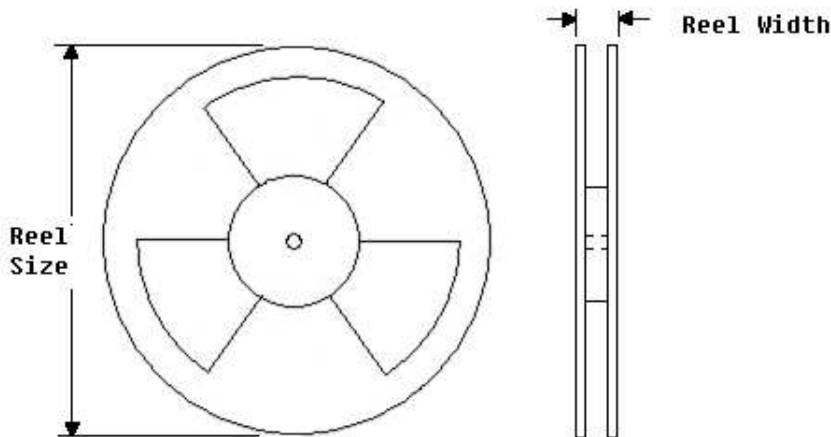
### 1. Taping orientation

QFN2x2



Feeding direction →

### 2. Carrier Tape & Reel specification for packages



| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Reel width(mm) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---------------|-----------------|------------------|------------------|----------------|--------------------|--------------------|--------------|
| QFN2x2        | 8               | 4                | 7"               | 8.4            | 400                | 160                | 3000         |

### 3. Others: NA